REMARKS

Claims 1 – 20 are pending in the application. Claims 1 and 10 have been amended.

Claims 1 – 8, 10 – 17 and 19 – 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hagersten et al. (US 5,710,907). Claims 9 and 18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hagersten, et al. in view of Arimili, et al. Claim 8 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Hagersten, et al as applied to Claim 1 and in view of Arimili, et al. While Applicant respectfully traverses these rejections, Claims 1 and 10 have nevertheless been amended for clarity.

Amended claim 1 recites in pertinent part "wherein a memory subsystem included in the node is configured to **select the translation function in response to the translation information** and to perform the translation function on the global address to generate a physical address...wherein in response to a request for access to the coherency unit, the additional memory subsystem is configured **to send the translation information** to the node." These features are neither taught nor suggested by Hagersten et al. or Arimilli et al., taken both singly and in combination.

In rejecting claim 1, the Examiner asserts that Hagersten et al. teaches a memory subsystem configured "to perform the translation function identified by the translation information on the global address to generate a physical address" at column 9, lines 17-32 and that Hagersten et al. further teaches that "the additional memory subsystem is configured to send the translation function to the node" at column 10, line 63 – column 11, line 7. Application respectfully disagrees. While Hagersten et al. discloses the mapping of different address spaces (column 9, lines 17-21) and performing translations of global addresses to LPAs (column 10, line 67 – column 11, line 2), Hagersten does not teach "wherein a memory subsystem included in the node is configured **to select** the translation function in response to the translation information and to perform the

translation function on the global address to generate a physical address." Furthermore, while Hagersten et al. discloses "sending the requested **data line** to global interface 315 of requesting sub-system 310 via global interconnect 390" (column 11, lines 6-8), Hagersten et al. does not teach "wherein in response to a request for access to the coherency unit, the additional memory subsystem is configured to send **the translation information** to the node." In accordance, claim 1 is believed to patentably distinguish over the cited references. Claim 10 recites similar features, and is likewise believed to patentably distinguish over the cited references.

Applicant further respectfully disagrees with many of the Examiner's characterizations and assertions with regard to dependent claims 2-9 and 11-20. However, in view of their dependency upon claims 1 and 10, respectively, these claims are believed to patentably distinguish over the cited references for at least the reasons stated above, and further elaboration is believed unnecessary.

CONCLUSION

Applicants submit the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5181-95501/BNK.

Respectfully submitted,

B. Noël Kivlin
Reg. No. 33,929
ATTORNEY FOR APPLICANT(S)

Meyertons, Hood, Kivlin,
Kowert, & Goetzel, P.C.
P.O. Box 398
Austin, TX 78767-0398
Phone: (512) 853-8800

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